AMENDMENTS TO THE CLAIMS

1. (Previously Presented) A semiconductor package comprising:

a plurality of leads, each of the leads defining:

a first surface;

a second surface disposed in opposed relation to the first surface; and

a third surface disposed in opposed relation to the second surface, the first surface being oriented between the second and third surfaces;

a first semiconductor die defining opposed first and second surfaces and including a plurality of bond pads disposed on the first surface thereof, portions of the first surface of the first semiconductor die being directly attached to the second surface of each of the leads such that each of the bond pads of the first semiconductor die is located between a respective pair of the leads so that the bond pads of the first semiconductor die do not contact the second surface of any one of the leads;

a second semiconductor die defining opposed first and second surfaces and including a plurality of bond pads disposed on the second surface thereof, the first surface of the second semiconductor die being attached to the second surface of the first semiconductor die;

a plurality of conductive connectors electrically connecting the bond pads of the first and second semiconductor dies to respective ones of the leads; and

an encapsulating portion applied to and at least partially encapsulating the leads, the first and second semiconductor dies, and the conductive connectors.

2. (Original) The semiconductor package of Claim 1 wherein the conductive connectors comprise conductive wires.

3. (Previously Presented) The semiconductor package of Claim 1 wherein:

the conductive connectors comprise first and second conductive wires;

the bond pads of the first semiconductor die are electrically connected to respective ones of the first surfaces of the leads by the first conductive wires; and

the bond pads of the second semiconductor die are electrically connected to respective ones of the second surfaces of the leads by the second conductive wires.

4. (Original) The semiconductor package of Claim 1 further comprising:

a die paddle defining opposed top and bottom surfaces, the leads being disposed about the die paddle;

the first surface of the first semiconductor die further being attached to the top surface of the die paddle.

5. (Original) The semiconductor package of Claim 4 wherein:

the first surface of the first semiconductor die is attached to the second surface of each of the leads and to the top surface of the die paddle by a first bonding means; and

the first surface of the second semiconductor die is attached to the second surface of the first semiconductor die by a second bonding means.

6. (Original) The semiconductor package of Claim 4 wherein:

the die paddle is formed to have a die paddle thickness;

each of the leads is formed to have a lead thickness between the second and third surfaces thereof; and

the die paddle thickness is substantially equal to the lead thickness.

7. (Original) The semiconductor package of Claim 4 wherein the encapsulating portion is applied to the die paddle such that the bottom surface of the die paddle is exposed within the encapsulating portion.

8. (Original) The semiconductor package of Claim 7 wherein the encapsulating portion is applied to the leads such that the third surface of each of the leads is exposed within the encapsulating portion.

9. (Original) The semiconductor package of Claim 1 wherein the encapsulating portion is applied to the leads such that the third surface of each of the leads is exposed within the encapsulating portion.

10. (Cancelled)

11. (Currently Amended) The semiconductor package of Claim ~~10~~ 1 wherein:

the first semiconductor die defines a peripheral edge; and

the conductive connectors electrically connecting the bond pads of the first semiconductor die to the leads are oriented inwardly relative to the peripheral edge of the first semiconductor die.

12-18. (Cancelled)

19. (Previously Presented) A semiconductor package comprising:

a plurality of leads;

a first semiconductor die including a plurality of bond pads disposed thereon, the first semiconductor die being directly attached to each of the leads such that each of the bond pads of the first semiconductor die is located between a respective pair of the leads so that the bond pads of the first semiconductor die do not contact any of the leads;

a second semiconductor die including a plurality of bond pads disposed thereon, the second semiconductor die being attached to the first semiconductor die;

means for electrically connecting the bond pads of the first and second semiconductor dies to respective ones of the leads; and

an encapsulating portion applied to and at least partially encapsulating the leads, the first and second semiconductor dies, and the electrical connection means.

20. (Previously Presented) The semiconductor package of Claim 19 wherein the electrical connection means comprises conductive wires.

21. (Previously Presented) The semiconductor package of Claim 20 wherein:

each of the leads defines opposed first and second surfaces and a third surface which is opposed to the second surface, the first surface being oriented between the second and third surfaces;

the bond pads of the first semiconductor die are electrically connected to respective ones of the first surfaces of the leads by first conductive wires; and

the bond pads of the second semiconductor die are electrically connected to respective ones of the second surfaces of the leads by second conductive wires.

22. (Previously Presented) The semiconductor package of Claim 21 wherein the encapsulating portion is applied to the leads such that the third surface of each of the leads is exposed within the encapsulating portion.

23. (Previously Presented) The semiconductor package of Claim 19 further comprising:

a die paddle, the leads being disposed about the die paddle;

the first semiconductor die being attached to the die paddle.

24. (Previously Presented) The semiconductor package of Claim 23 wherein:

the die paddle defines opposed top and bottom surfaces, with the first semiconductor die being attached to the top surface of the die paddle; and

the encapsulating portion is applied to the die paddle such that the bottom surface of the die paddle is exposed within the encapsulating portion.

25. (Cancelled)